

- 3 (a) loading a first vector into a first register, said first vector comprising a
4 plurality of N-bit elements;
5 (b) loading a second vector into a second register, said second vector
6 comprising a plurality of N-bit elements;
7 (c) executing an arithmetic instruction for at least one pair consisting of an
8 N-bit element in said first register and an N-bit element in said second register, to produce a
9 resulting element;
10 (d) writing said resulting element into an M-bit element of an accumulator,
11 wherein M is greater than N;
12 (e) transforming said resulting element in said accumulator into a width of
13 N-bits; and
14 (f) writing said resulting element into a third register.

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1 ²~~42~~. The method as recited in claim ¹~~41~~, wherein said accumulator comprises a plurality of M-
2 bit elements and wherein steps (c)-(f) operate on a plurality of elements of said first and second
3 vectors to produce a resultant vector formed from a plurality of resulting elements written to said
4 third register.

1 ³~~43~~. The method as recited in claim ²~~42~~, further comprising a step before step (c) of:
2 selecting an element from said second register; and
3 copying said element into all other elements in said second register.

1 ⁴~~44~~. The method as recited in claim ³~~43~~, further comprising a step before step (f) of:
2 selecting a subset of said resulting elements in said accumulator for writing to said
3 third register, said subset being chosen from any one of: the low third bits, the middle third bits,
4 and the high third bits of said resulting elements in said accumulator.

1 ⁵~~45~~. The method as recited in claim ⁴~~44~~, wherein M is equal to three times N.

1 ⁵~~46~~. The method as recited in claim ⁵~~45~~, wherein N is equal to eight or sixteen.

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Sub D1 1⁸ 47. The method as recited in claim ~~42~~², wherein said resulting elements in said accumulator are wrapped around the representable range of said resulting elements.

1 ~~48~~⁸ 48. The method as recited in claim ~~42~~², further comprising a step before step (f) of:
2 dividing said resulting elements stored in said accumulator into a plurality of
3 subsets;
4 writing each subset to at least one of a plurality of registers, each of said plurality
5 of registers having a width smaller than said accumulator width.

B1 1 ~~49~~⁹ 49. The method as recited in claim ~~41~~¹, wherein said loading step (a) and said loading step (b)
2 are not formatted.

1 1⁰ 50. The method as recited in claim ~~41~~¹, further comprising a step before step (d) of:
2 formatting said resulting element as specified in said arithmetic instruction.

1 1¹ 51. The method as recited in claim ~~41~~¹, wherein said arithmetic instruction is any one of:
2 addition, multiplication and subtraction.

1 1² 52. The method as recited in claim ~~41~~¹, wherein step (e) comprises the steps of:
2 shifting said resulting element in said accumulator for scaling the value of said
3 resulting element;
4 rounding said resulting element; and
5 clamping said resulting element.

Sub D2 1 1³ 53. The method as recited in claim ~~52~~¹², wherein said rounding step comprises one of:
2 rounding said resulting element towards zero;
3 rounding said resulting element towards the nearest unit, wherein said resulting
4 element is rounded away from zero if said resulting element is at least halfway towards the
5 nearest unit; and
6 rounding said resulting element towards the nearest unit, wherein said resulting
7 element is rounded towards zero if said resulting element is at least halfway towards the nearest
8 unit.

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- 1 ¹⁴~~54~~. The method as recited in claim ~~41~~¹, further comprising a step before step (d) of:
2 adding an element previously stored in said accumulator to said resulting element.
- 1 ¹⁵~~55~~. The method as recited in claim ~~41~~¹, wherein N is any one of: eight, sixteen, thirty-two and
2 sixty-four.
- 1 ¹⁶~~56~~. The method as recited in claim ~~55~~¹⁵, wherein said N-bit elements are integers.
- 1 ¹⁷~~57~~. The method as recited in claim ~~55~~¹⁵, wherein each of said first and second vectors has a
2 width of 64 bits.
- 1 ¹⁸~~58~~. The method as recited in claim ~~57~~¹⁷, wherein said accumulator is a register having a width
2 equal to an integer multiple of 64 bits.
- 1 ¹⁹~~59~~. The method as recited in claim ~~58~~¹⁸, wherein said accumulator is a register having a width
2 of 192 bits.
- 1 ²⁰~~60~~. The method as recited in claim ~~41~~¹, wherein said first register, said second register, and
2 said third register are floating point registers.
- 1 ²¹~~61~~. The method as recited in claim ~~41~~¹, wherein said first register, said second register, and
2 said third register each have a width of 64-bits.
- 1 ²²~~62~~. A processor for providing extended precision in single instruction multiple data (SIMD)
2 arithmetic operations, comprising:
3 means for executing an arithmetic instruction involving an element of a first
4 vector and an element of a second vector to produce a resulting element, said first and second
5 vector comprising a plurality of N-bit elements;
6 an accumulator for receiving said resulting element, wherein said resulting
7 element is stored in an M-bit element of said accumulator and wherein M is greater than N;

8 means for transforming said resulting element in said accumulator into a width
9 of N-bits; and
10 means for writing said transformed resulting element to a register.

1 ²³~~63~~. The processor as recited in claim ²²~~62~~, wherein said accumulator comprises a plurality of
2 M-bit elements and wherein said means for executing is repeated for said plurality of elements
3 of said first and second vectors to produce a plurality of resulting elements that are received by
4 said accumulator and wherein said means for transforming and said means for writing are
5 performed on said plurality of resulting elements. D

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1 ²⁴~~64~~. The processor as recited in claim ²³~~63~~, wherein means for writing comprises:
2 selecting a subset of said resulting elements in said accumulator for writing to said
3 register, said subset being chosen from any one of: the low third bits, the middle third bits, and
4 the high third bits of said resulting elements in said accumulator.

1 ²⁵~~65~~. The processor as recited in claim ²³~~63~~, wherein M is equal to three times N.

1 ²⁶~~66~~. The processor as recited in claim ²⁵~~65~~, wherein N is equal to eight or sixteen.

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2 ²⁷~~67~~. The system as recited in claim ²³~~63~~, wherein said resulting elements in said accumulator
are wrapped around the representable range of said resulting elements.

1 ²⁸~~68~~. The system as recited in claim ²³~~63~~, further comprising:
2 dividing said resulting elements stored in said accumulator into a plurality of
3 subsets;
4 writing each subset to at least one of a plurality of registers, each of said plurality
5 of registers having a width smaller than said accumulator width.

1 ²⁹~~69~~. The system as recited in claim ²²~~62~~, further comprising:
2 means for formatting said resulting element in said accumulator as specified in
3 said arithmetic instruction. D

1 ³⁰~~20~~. The processor as recited in claim ²²~~62~~, wherein said arithmetic instruction is any one of:
2 addition, multiplication and subtraction.

1 ³¹~~21~~. The processor as recited in claim ²²~~62~~, wherein means for transforming comprises:
2 means for shifting said resulting element in said accumulator for scaling the value
3 of said resulting element;
4 means for rounding said resulting element; and
5 means for clamping said resulting element.

1 ³²~~22~~. The processor as recited in claim ³¹~~21~~, wherein said rounding means comprises one of:
2 means for rounding said resulting element towards zero;
3 means for rounding said resulting element towards the nearest unit, wherein said
4 resulting element is rounded away from zero if said resulting element is at least halfway towards
5 the nearest unit; and
6 means for rounding said resulting element towards the nearest unit, wherein said
7 resulting element is rounded towards zero if said resulting element is at least halfway towards
8 the nearest unit.

1 ³³~~23~~. The processor as recited in claim ²²~~62~~, further comprising:
2 means for adding an element previously stored in said accumulator to said
3 resulting element, upon reception of said resulting element by said accumulator.

1 ³⁴~~24~~. The processor as recited in claim ²²~~62~~, wherein N is any one of: eight, sixteen, thirty-two
2 and sixty-four.

1 ³⁵~~25~~. The processor as recited in claim ³⁴~~24~~, wherein said N-bit elements are integers.

1 ³⁶~~26~~. The processor as recited in claim ³⁴~~24~~, wherein each of said first and said second vectors
2 has a width of 64 bits.

1 ³⁷~~27~~. The processor as recited in claim ³⁶~~26~~, wherein said accumulator is a register having a
2 width equal to an integer multiple of 64 bits.